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OPTICAL MARGIN TESTING SYSTEM FOR AUTOMATIC POWER CONTROL LOOPS

Field of the Invention

The present invention relates generally to the data processing field, and more particularly, relates to an optical margin testing system for automatic power control loops.

Description of the Related Art

During manufacture of products, it is desirable to provide margin testing in order to provide a more reliable product. It is desirable to minimize the number of required test inputs to the product being tested, while executing multiple margin testing functions. It is desirable to implement margin testing without requiring complex software control or readjusting any bias control potentiometers.

For many types of laser-based optical products, typically automatic power control loops are utilized. In optical margin testing for automatic power control loops it is desirable to both increase and decrease the operating point of the light emitting device to validate signal integrity margins. It is desirable to both increase and decrease the operating point of automatic power control loop, for example, by a set percentage threshold to validate signal integrity margins.

A need exists for an optical margin testing system for automatic power control loops. It is desirable to provide such an optical margin testing

system for automatic power control loops that provides effective performance and that is simple to implement.

Summary of the Invention

A principal object of the present invention is to provide an optical margin testing system for automatic power control loops. Another important object of the present invention is to provide such an optical margin testing system for automatic power control loops substantially without negative effect.

In brief, an optical margin testing system is provided for automatic power control loops. An optical circuit includes a laser diode and a monitor diode coupled to an automatic power control loop. A bias generator circuit generates a control signal. The control signal is applied to the automatic power control loop. The control signal enables an operation point of the laser diode to both increase and decrease by a set percentage value for optical margin testing.

In accordance with features of the invention, the bias generator circuit includes a tri-state receiver. An input signal is applied to the tri-state receiver for selecting one of a normal operational mode, an increased set percentage value operational mode, and a decreased set percentage value operational mode. A current mirror is coupled to the tri-state receiver and provides the control signal that is applied to the automatic power control loop.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. 1 is a schematic and block diagram illustrating an optical margin testing system for automatic power control loops in accordance with the preferred embodiment; and

FIG. 2 is a chart illustrating operation of the optical margin testing system of FIG. 1 including possible values of a margin control input signal applied to a tri-state receiver of the optical margin testing system of FIG. 1 to selectively provide optical margin testing control outputs in accordance with the preferred embodiment.

Detailed Description of the Preferred Embodiments

Having reference now to the drawings, in FIG. 1 there is shown an exemplary optical margin testing system for automatic power control loops in accordance with the preferred embodiment generally designated by the reference character 100. As shown in FIG. 1, optical margin testing system 100 provides a control signal for optical margin testing an automatic power control (APC) loop 102.

In accordance with features of the preferred embodiment, the operating point of the automatic power control loop 102 is shifted without requiring any software control or readjusting any bias control potentiometers. Optical margin testing system 100 effectively implements a 2-bit switched current source into an APC loop 102 so that when the appropriate control signal is provided, the bias generator can increase or decrease the operating point by a defined percentage X%. A single I/O using a tri-state receiver 104 where the three states are normal mode, +X% mode, and -X% mode provides the control signal.

Optical margin testing system 100 includes the tri-state receiver 104 having an input labeled MARGIN. The tri-state receiver 104 is coupled to a programmable current mirror 106 of the optical margin testing system 100.

The MARGIN input is selectively provided as one of zero, high impedance, or one. The MARGIN input is provided as zero for a normal operational mode, as high impedance for an increased +X% operational mode, and as one for a decreased -X% operational mode. A state table of operation of optical margin testing system 100 is illustrated and described with respect to FIG. 2.

Programmable current mirror 106 includes a current input I_{IN} and

provides a current output I_{OUT}. The current output I_{OUT} is applied to the automatic power control (APC) loop 102 as indicated at a line labeled I_{APCOUT}. The current input I_{IN} is applied to the programmable current mirror 106 as indicated at a line labeled I_{APC} by an input current generating circuit generally designated by 108. Input current generating circuit 108 includes an operational amplifier 110 coupled to a gate input of a field effect transistor 112, such as an N-channel field effect transistor (NFET) 112. NFET 112 is connected between the current input I_{IN} of programmable current mirror 106 and a variable resistor R_{APC} 114. A voltage reference V_{REF} is applied to a first input + of operational amplifier 110. The junction connection of NFET 112 and variable resistor R_{APC} 114 is connected to a second input - of operational amplifier 110.

As shown in FIG. 1, input current generating circuit 108 generates the current mirror input bias current I_{APC} by controlling a virtual voltage across the variable resistor 114. The V_{REF} voltage applied to operational amplifier 110 is reflected across the variable resistor R_{APC} 114. This generates the current mirror input bias current I_{APC} that is substantially equal to V_{REF} / R_{APC}. This current I_{APC} is mirrored and the mirrored current I_{APCOUT} is applied to the APC loop 102 for comparison with a feedback current to the APC loop 102.

A monitored optical circuit generally designated by 120 includes a laser diode 122 and a monitor diode or photodiode 124. A bias current as indicated at a line labeled BIAS CURRENT is applied to the laser diode 122 via the APC loop 102. The feedback current from the monitor photodiode 124 as indicated at a line labeled FEEDBACK CURRENT is applied to the APC loop 102

In accordance with features of the preferred embodiment, the optical margin testing system 100 implements simple selectable scaled current sources which make use of existing adjustment resistors for optical margin testing. Optical margin testing system 100 provides a single I/O interface to execute the margin testing functions to both increase and decrease the operating point of automatic power control loop 102 by the set percentage threshold X% to validate signal integrity margins. Optical margin testing system 100 delivers an accurate representation of the slight deviation from

the normal operating point of the laser diode 122.

Referring also to FIG. 2, the implementation of the invention is contained in the programmable current mirror 106. The state table of operation is illustrated in FIG. 2 and described in the following Table 1. To implement this function, a simple combination of scaled current sources that are selectable by the +x% and –x% control signals will achieve the desired output.

Table 1

Margin	+X%	-X%	I_{OUT} / I_{IN}
0	0	0	k*1
HighZ	1	0	k*(1+X%)
1	0	1	k*(1-X%)

Optical margin testing system 100 enables effective margin testing of a product including monitored optical circuit 120 before sending the product out into the field. Optical margin testing system 100 enables the operating point of the light emitting device 122 to be skewed slightly to validate signal integrity margins effected by modulating near the threshold or near the Pmax (maximum power due to saturation of optical assembly) of the light emitting device. The +X% is small enough to be contained under the laser eye safety limits but large enough to provide a sufficient stress of the laser device 122.

An advantage of the optical margin testing system 100 is that a fixed value of the variable resistor 114 is used. This is a significant improvement over testing arrangements that require changing a variable resistor or potentiometer value to skew an operating point for an optical circuit being tested.

It should be understood that the present invention is not limited to the

exemplary optical margin testing system 100 including the programmable current mirror 106 as shown in FIG. 1. For example, scaled voltage sources, for example, multiplexed to the V_{REF} node, could be used to both increase and decrease the operating point of automatic power control loop 102 by the set percentage threshold X% to validate signal integrity margins.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.